Technology Transfer in Computing Systems

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TETRACOM D3.32: Power aware multicore software mapping

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Technical achievements in the last decade had awoken everyone's desire of possessing powerful mobile devices to be connected to everyone everywhere. The resulting ever increasing computational workload combined with tighter power budgets – due to heat issues and battery lifetime – enforces new design decisions for hardware and software. Especially in the context of upcoming 5G mobile networks, heterogeneous multi- and many-processor systems on chip (MPSoC) composed of different core architectures are seen as solution exploiting the advantages of MPSoCs. However, one of the biggest hurdles to exploit multicore architectures from the software side is how to efficiently develop performance and power co-optimized parallel software.

Silexica Software Solutions GmbH is a VC-backed spin-off from RWTH ICE, focused on producing novel compiler technology and tools for programming embedded multicore platforms. The tool suite comprises SLX Parallelizer, SLX Mapper, and SLX Generator. SLX Mapper generates an optimized spatial and temporal allocation of SW tasks on the processing elements of heterogeneous MPSoCs. The purpose of the TTP is to investigate the use of RWTH ICE's electronic system-level (ESL) power estimation methodology for processor, on-chip interconnect, and other SoC components. The general goals are to adapt and extend the power estimation technology for Silexica´s environment. By integrating the technology into the SLX mapper, power aware software mapping is enabled. Please note that this TTP covers partially the period of the whole collaboration project between RWTH and Silexica.

The ESL power estimation methodology starts from an ESL system containing a model of the component for which a power model shall be created. Inside the ESL system, all available information, e.g. instructions executed by a processor or number of accessed data, is traced and used as input for the power model. Additionally, a reference power trace of this component has to be obtained. Possible options for obtaining this reference power trace are power simulation on lower levels like gate or layout level and power measurements using real hardware. The methodology takes the available power information from the reference power trace and back-annotates it to the ESL model, i.e. create an ESL power model for the component. This back-annotation, or more precisely calibration is the method of determining the coefficients of a linear power model from a reference scenario. For this calibration scenario, different methods can be used to compute the coefficients. A simple approach is minimizing the mean squared error. More sophisticated approaches like non-negative least-squares algorithms exist as well. Several case studies have shown power estimation errors with less than 5%.

In the TTP, the ESL power estimation methodology is integrated into the SLX Mapper. Major adaptions are the choice of input data for the linear power model. Inside the SLX Mapper, the performance analyzer offers an instruction mix which has to be annotated with timing information. The instruction mix serves as input for the linear power model. Enabling power estimation for the SLX Mapper is the important step for the subsequent tasks. During the TTP, power models are created for different processor types, e.g., ARM Cortex A7, A9, A15 and Blackfin 609 DSP. Based on the power modeling capability, a novel power aware software mapping algorithm is deployed to develop performance and power co-optimized parallel software. This algorithm is used for, e.g., a specific SoC platform from Silexica's customers to determine power and energy saving potentials. While the final results of the project are still in the making, in the TTP phase, RWTH has successfully delivered the power estimation methodology and supported the integration into the SLX Mapper as well as the creation of processor power models and a customer specific power aware SoC platform.