



FP7 Coordination and Support Action to fund 50 technology transfer projects (TTP) in computing systems. This project has received funding from the European Union's Seventh Framework Programme for research, technological development and demonstration under grant agreement n° 609491.

## FPGA Acceleration of Short Read Alignment

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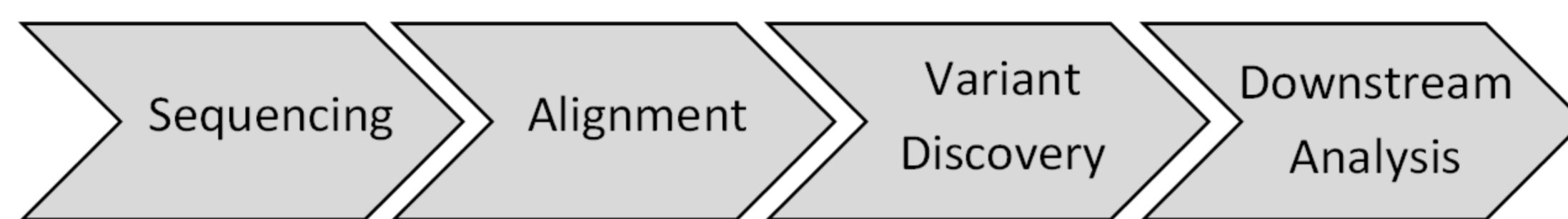
### TTP Problem

NGS throughput increasing faster than Moore's Law



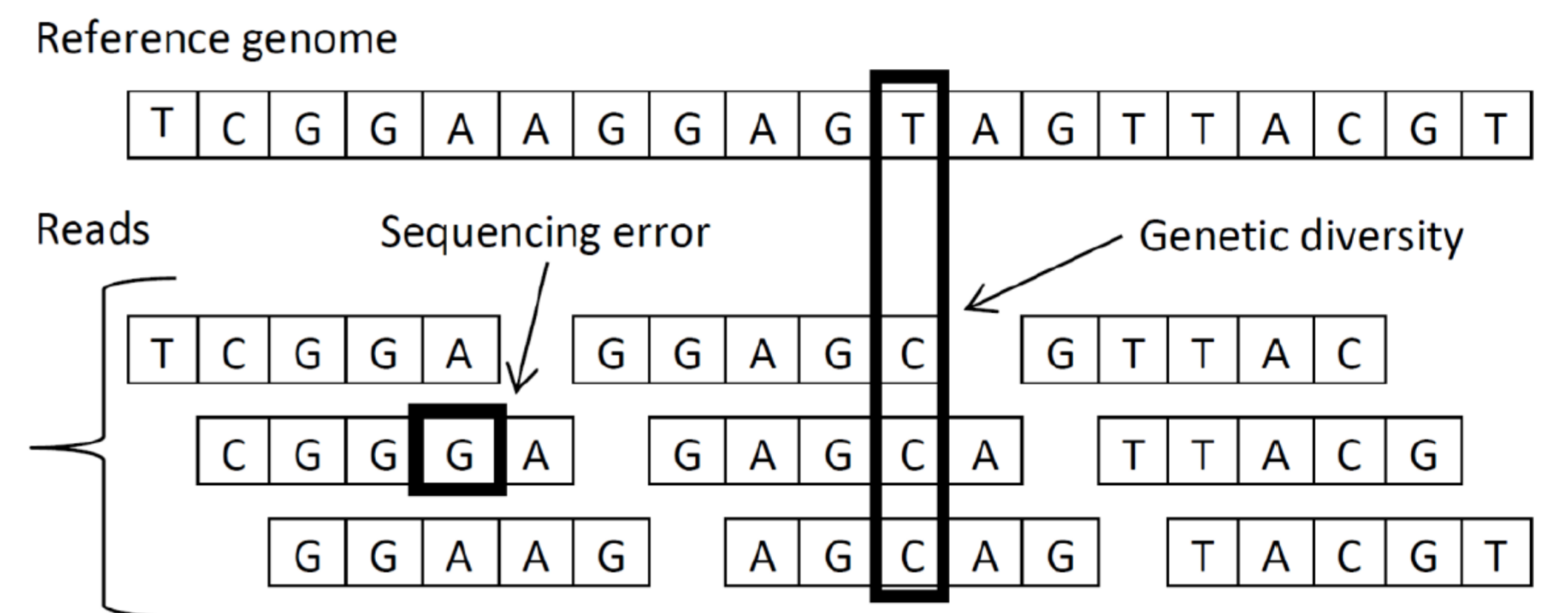
Over 200GB of data to analyse per run

NGS analysis can take days to perform



Alignment is a bottleneck in NGS pipelines: accounts for over 50% of analysis time

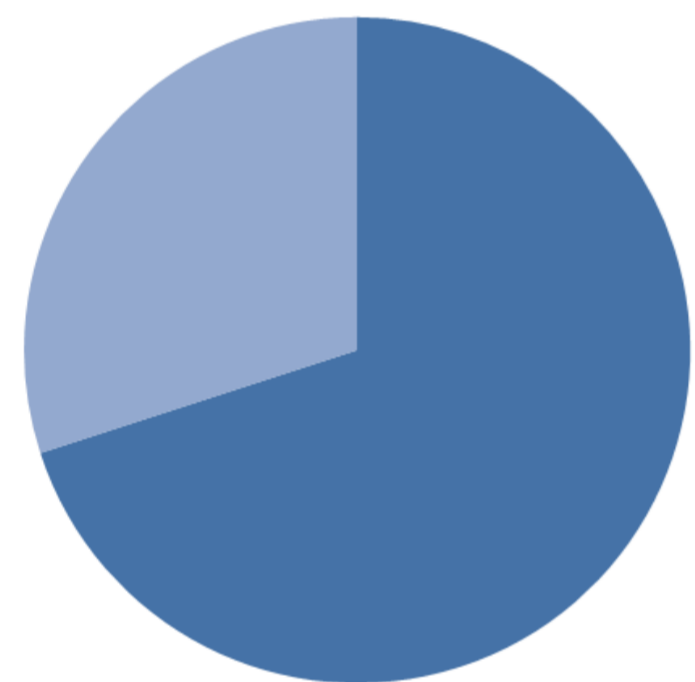
Map sequenced reads to positions in known reference genome



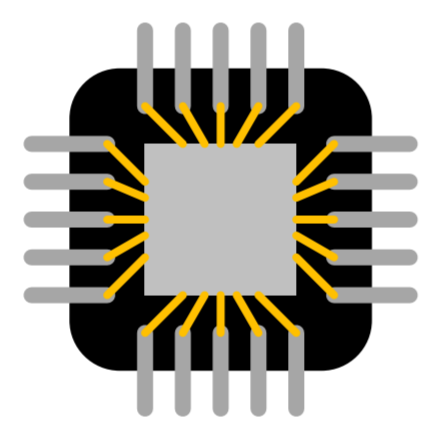
Both exact and approximate alignment required

### TTP Solution

Over 70% of reads can be exactly aligned to reference



Develop customised hardware architecture for exact alignment



Hardware Module

#### Algorithm Design

Design based on FM-index

Develop optimisations to reduce off-chip memory access:

- n-step FM-index
- Index oversampling

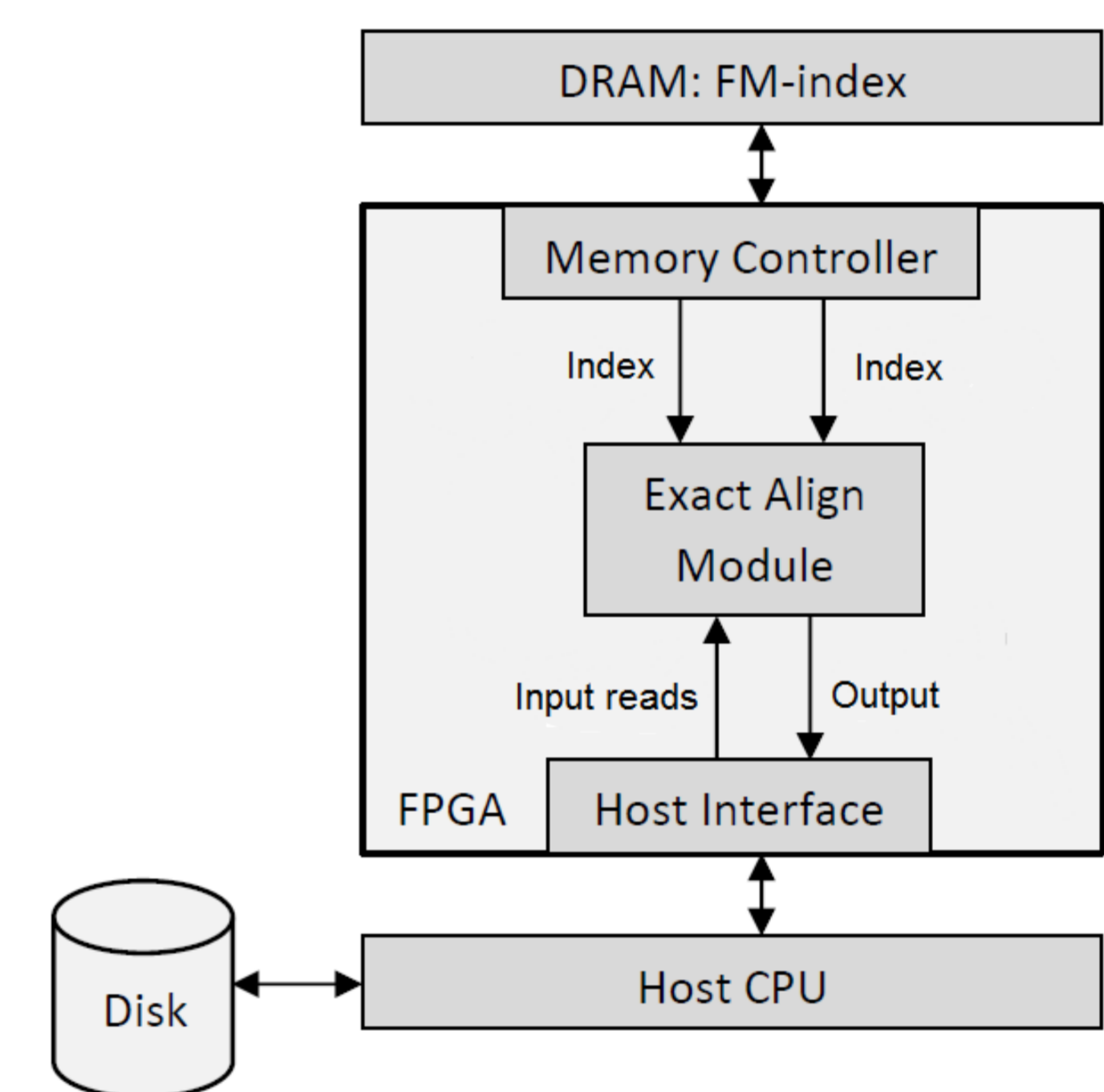
#### Hardware Design

Implement using Vivado HLS

Develop optimisations to improve hardware performance:

- Interleave processing of multiple reads
- Reduce resource usage

#### Hardware Design Overview



Derive equations to estimate module performance for hardware platforms



### TTP Impact

#### Benchmarking

Software tools

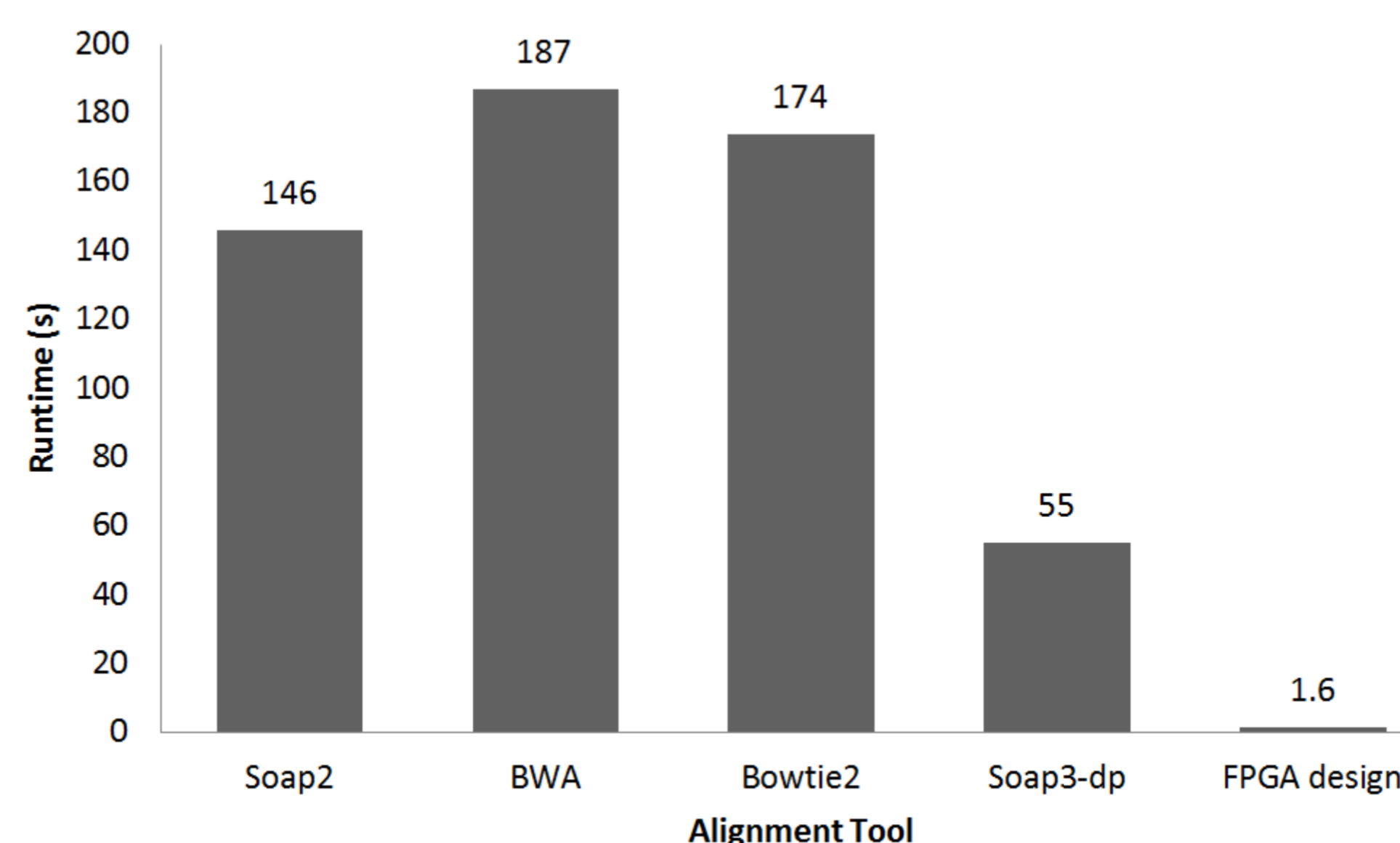
- Soap2, BWA, Bowtie2 – Dual Intel Xeon
- Soap3-dp – NVIDIA C2070 GPU

Hardware Design

- Convey HC-2ex with 4 Xilinx Viretx-6 LX760 FPGAs

Data set

- 10M reads of 100 bases from Hg19



#### Results

Hardware performance up to:

- 91x faster than Soap2
- 34x faster than Soap3-dp

Implications

- Alignment reduced from hours to minutes

### TTP Facts

Contact: James Arram  
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