Technology Transfer in Computing Systems

D3.1: Individual TTP1 abstract

Project no.:	609491
Funding scheme:	Collaborative project
Start date of the project:	1st September 2013
Duration:	36 months
Work programme topic:	FP7-ICT-2013-10
Deliverable type:	Report
Deliverable reference number:	ICT-609491 / D3.1
WP and tasks contributing:	WP 3 / all
Due date:	31/07/2014
Actual submission date:	31/07/2014
Responsible Organization:	RWTH
Dissemination Level:	Public
Revision:	1.0

TETRACOM D3.1: System-level Power Estimation for SoC Platforms

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Advances in CMOS technology enabled the integration of complex systems with multiple processors on a single chip. Those Multiprocessor Systems on Chip (MPSoCs) try to satisfy the demand for more and more computational performance in embedded systems. One of the biggest obstacles for further integration of those MPSoCs is the dissipation of the heat generated due to the power consumption. Therefore, it is essential to consider power consumption of a new MPSoC design already during early design space exploration, which usually is done at Electronic System Level (ESL).

Because standard ESL tools like SystemC allow only to simulate the functionality and the timing of a system, an ESL power estimation methodology has been developed at RWTH. This methodology allows to create ESL power models for existing SystemC models based on a reference scenario for which the power consumption curve over time is known. The power model will compute the power estimate as a linear combination of traces recorded by instrumentation inserted into the model. The linear factors are *calibrated* using the reference scenario. Once the models in the ESL library have been power-extended, they can be used to simulate new designs including their power consumption.

In this technology transfer project, the existing power estimation methodology has been improved to support the requirements of Futurewei Technologies, so it is suitable for integration into their ESL workflow. The improvements are described in the following.

Power Model Calibration using Power Measurements

The existing methodology relied on low-level (e.g. post-layout gate-level) simulations to obtain the power consumption curve of the reference scenarios. Futurewei was in need of power estimation for a processor model for which no low-level model was available. Therefore, the methodology has been extended to support hardware measurements for obtaining the reference power curves.

While low-level simulations are cycle-accurate and deliver a power consumption value in each cycle, the reference power curve obtained via hardware measurements has a lower granularity. Compared to a cycle-accurate power trace, the measured power trace is low-pass filtered and sampled with a certain period. This required to adapt the recording of traces from inside the model to accumulate events during the sampling period and output a value at its end, so the traces have got the same resolution as the reference power curve.

Power Model Calibration under Timing Mismatch

The ESL platform model used in this project does not model the timing behavior of the reference platform perfectly. The timing deviates up to +/-50% depending on the scenario. This leads to traces obtained from inside the model having a different length than the reference power curve obtained from the hardware. As the power model calibration has to compare the traces to the reference power curve at each sampling location, the traces have to be converted to have the same length. The project has shown that linear scaling in time can be used for this conversion.

Development of a Power Model for the ARM Cortex A9 Processor and Evaluation

A power model for the ARM Cortex A9 processor has been created based on the ARM out-of-order model contained in the gem5 simulation framework. The reference power curves have been measured from the ARM Cortex A9 cores in the TI OMAP4460 chip on the PandaBoard ES.

Leave-one-out cross validation of power models has been performed over a set of benchmarks containing dhrystone, lte-benchmark, mibench telecomm, streamit and wibench. The relative root mean square (RMS) power estimation error is about 11% on average. The worst case error is about 63%, but this is only one out of three cases where the error is larger than 26%.

Constraining the factors in the power models to non-negative values during calibration improves the quality of the created power models. The average RMS error is reduced to about 5%. All errors except for the worst case error of 36% are below 13%.