Technology Transfer in Computing Systems

D3.27: Individual TTP27 abstract

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TETRACOM D3.27: IP DIME: Image Processing to Detect Hidden Defects in Manufactured Electronics Systems

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Modern electronic systems are becoming ever smaller and more difficult to test and inspect. The recent advances towards 3D chip technology with multi-die and many layered devices demands new methods for inspection and reliability testing. Roadmaps such as ITRS have indicated that new methods for metrology to test manufactured devices are urgently required. For defect detection throughout the lifetime of automotive electronics systems is difficult and provides challenges to maintain the reliability required by the public to help exceed customer expectations.

The main objectives in this work were the integration of 2D and 3D acoustic image processing algorithms in order to speed up failure detection and analysis execution times in validation and test labs. The expected added value from the technology transfer will be to turn academic research outputs into new tools for failure analysis labs to validate the integrity of manufactured electronics systems. Secondary objectives were to assess the optimum accuracy of the algorithms for the measurement of solder joint failures, failure initiation and lifetime degradation to failure. This shall help inform future electronics design, manufacturing and prognostics research, thereby enabling increased product reliability.

In this TTP, the focus was to further investigate through-life reliability testing of flip chip solder joints, attempting to track and estimate times to failure. The benefits of the work completed are:

- Accurate assessment of thermally induced failures through acoustic and X-ray analysis.
- Lifetime assessment and understanding of solder joint behavior by position on a chip and the chips position on the floorplan of a PCB. This included double-side populated PCBs with back-to-back and off-set chip positions to help mimic various possible in service failure modes.

Delphi is a leading tier 1 automotive electronics company supplying products to many world markets. The company designs, manufactures and validates electronic products for many applications in vehicle control, infotainment and driver safety. If products can be validated more quickly whilst maintaining the confidence of long term reliable operation, both consumer and companies will win. Costs will be reduced without compromising reliability, through savings in time and energy.

Demonstration of typical reliability results are represented for 109 ball rectangular flip chips. Chips U35 and U39 soldered onto the underside of a FR4 PCB overlapped by 50% by similar flip-chips on the top side of the PCB. The more reliable connections close to the centre of the chips took over 100 thermal cycles to failure, whereas the corner solder balls were amongst the first to fail at around 16 cycles. Figures 1 and 2 show the cycles to failure for Chips U35 and U39 for the aggressive thermal cycling tests applied. Figure 3 shows part of the design schematic for the PCB manufactured to investigate chip reliability with floorplan layout.

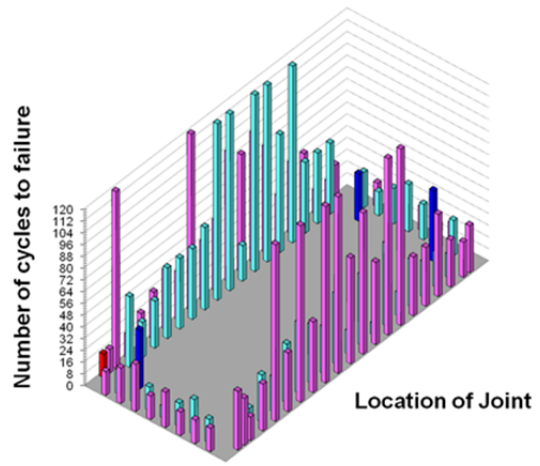

Figure 1 Number of cycles to failure for a flip chip U35 with 109 connections

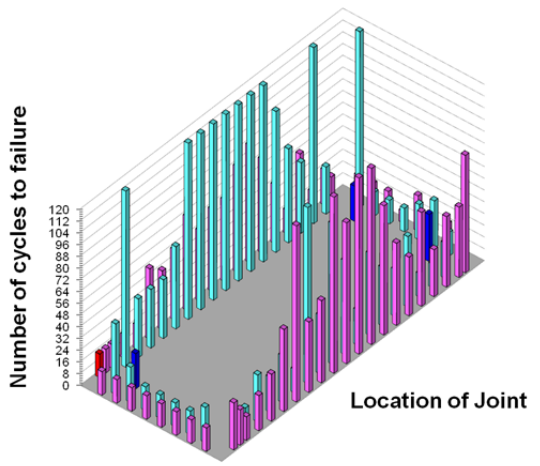

Figure 2 Number of cycles to failure for a flip chip U39 with 109 connections

Figures 1 and 2 were developed from acoustic scans of all solder joints after periods of 8 thermal cycles.

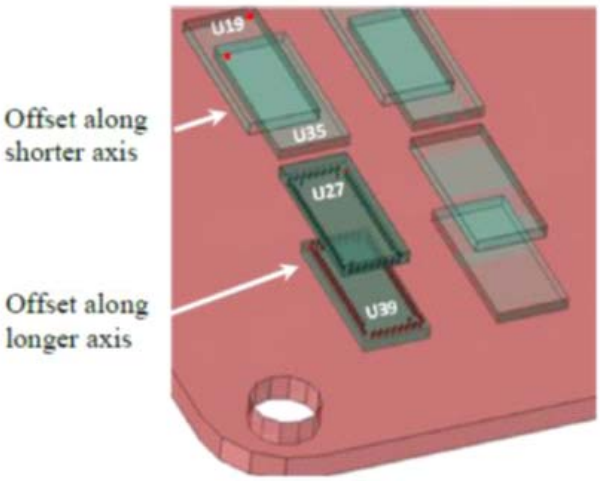

Figure 3 Chips U35 and U39 shown on the underside of a double mounted PCB schematic with chips off set between top and bottom sides on different axes

In the TTP, advice from Delphi has informed the Circuit Board Assembly (CBA) requirements, environmental testing and thermal profile conditions to induce the majority of solder joints to fail within 100 thermal cycles. Subsequent analysis of the through lifetime data opened up more food for thought as tracking of individual failures at a micro level is difficult. Further work with greater resolution and measurement accuracy at each cycle are proposed as a future project. Longer term the aim is to find and track the initiation of all cracks in solder bumps cycle-by-cycle to obtain a fuller understanding of long term reliability implications in products. This will be really useful for all validation labs in the future, saving test time money and providing cheaper and more reliable products to the consumer. Furthermore, this detailed understanding forms the fundamental core of work in the area of prognostics for electronics systems which is currently in its infancy.