An Advanced Turbo-Decoder IP for LTE-A

Stefan Weithoffer, Christian Weis, Norbert Wehn, University of Kaiserslautern, Germany
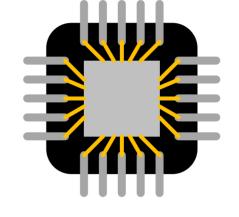Matthias Alles, Timo Lehnig-Emden, Creonic GmbH, Germany

TTP Problem

Today's Wireless Communication Standards require complex decoding architectures

TX

LTE FEC Turbo Encoder → Mapping → MIMO Modulator → OFDM → D/A

MAC Layer

LTE FEC Turbo Decoder ← Demapping ← MIMO Demodulator ← OFDM ← A/D

RX

FEC = Forward Error Correction

Availability of an Advanced Turbo Decoder IP for LTE-A

4G / 5G

Requirements

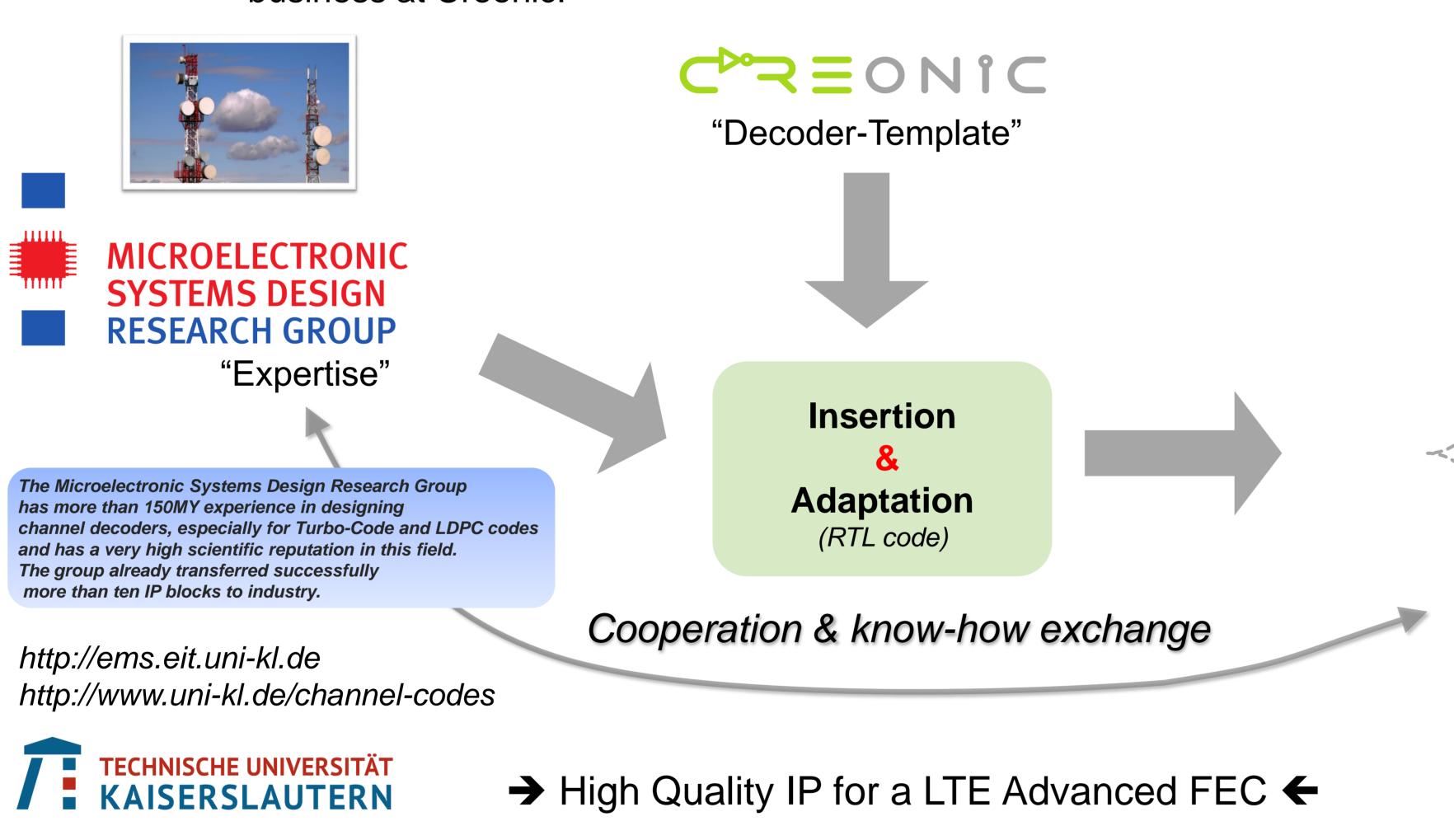Implementable on different Hardware Architectures

ASIC / FPGA

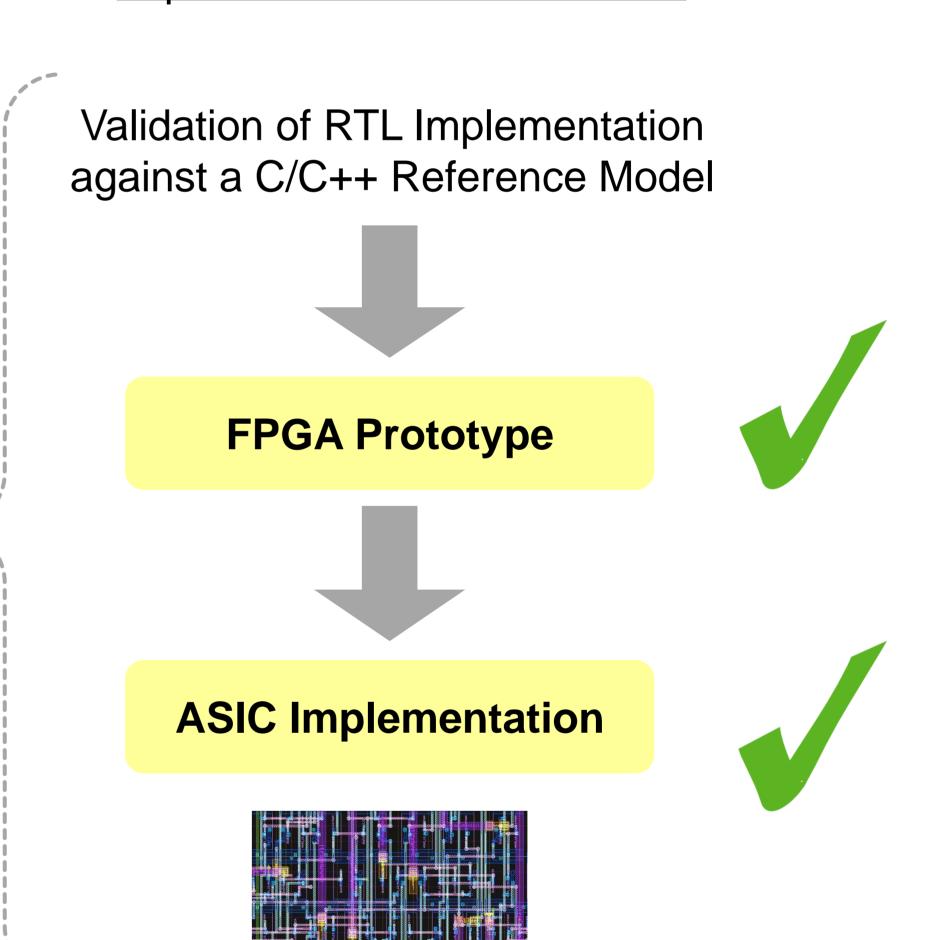Validated against the Wireless Standard Specifications

LTE, LTE-A, …

TTP Solution

Create with the existing know-how of Turbo-Decoders at the University of Kaiserslautern an IP suitable for enabling new business at Creonic:
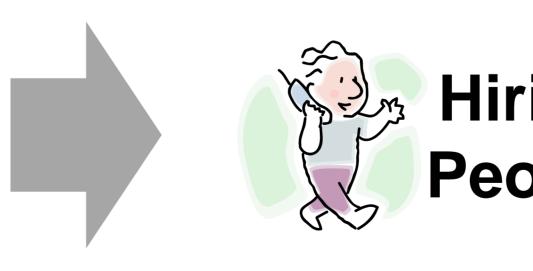
MICROELECTRONIC SYSTEMS DESIGN RESEARCH GROUP
"Expertise"

The Microelectronic Systems Design Research Group has more than 150MY experience in designing channel decoders, especially for Turbo-Code and LDPC codes and has a very high scientific reputation in this field. The group already transferred successfully more than ten IP blocks to industry.

http://ems.eit.uni-kl.de
http://www.uni-kl.de/channel-codes

TECHNISCHE UNIVERSITÄT KAISERSLAUTERN

CREONIC
"Decoder-Template"

Insertion & Adaptation
(RTL code)

Cooperation & know-how exchange

→ High Quality IP for a LTE Advanced FEC ←

Implementation and Validation

Validation of RTL Implementation against a C/C++ Reference Model
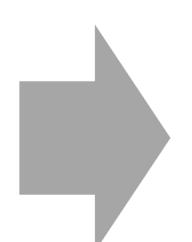
FPGA Prototype ✓

ASIC Implementation ✓

TTP Impact

4G / 5G LTE Advanced FEC: Competitive Advantages

- **Very high throughput FEC: > 1 Gbit/s**
- **Near ideal communications performance** even for high code rates ~ 1.0
- **Dynamic** reconfigurable **interleaver**
- Transport and code block **CRC checks**
- CRC driven iteration control, early stopping after each half-iteration
- Optional soft decision output for the complete code word
- **Scalable architecture** allows trade-offs between speed, throughput, resources and memory sharing
- **ASIC customers** in North America

Hiring People

1-3 new employers expected in the next 3 years

New Contracts

> 500,000 € expected revenue in the first 5 years

TTP Facts

MICROELECTRONIC SYSTEMS DESIGN RESEARCH GROUP

CREONIC
Creonic GmbH, Kaiserslautern, Germany

TECHNISCHE UNIVERSITÄT KAISERSLAUTERN