TETRACOM: Technology Transfer in Computing Systems

FP7 Coordination and Support Action to fund 50 technology transfer projects (TTP) in computing systems.
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eGPU Accelerated HEVC/H.265 Video Decoder

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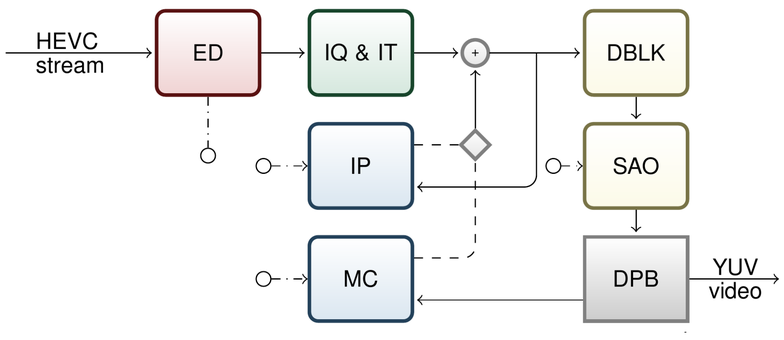
TTP Problem

Low-power HEVC/H.265 video decoding

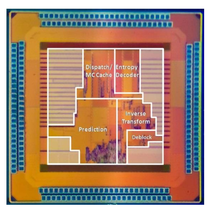


- Very low power: < 1 Watt
- Support other codecs, and codec extensions

Existing Methods

ASIC/ASIP

- Real-time ✓
- Low-power ✓
- Not flexible ✗
- Area overhead ✗



Source: Tikekar et al. JSSC, Jan 2014

CPU software

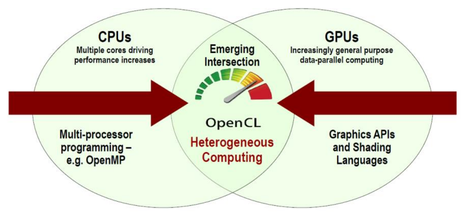
- Flexible prog. model ✓
- Power efficiency ✗
- High area, cost ✗

```
inline uint decodeBinEP( )
{
  m_iValue <<=1;
  if ( ++m_bitsNeeded == 0 ){
    refill();
  }
  int scaledRange = m_iRange << (CABAC_BITS-1);
  if ( m_iValue >= scaledRange ){
    m_iValue -= scaledRange;
    return 1;
  }
  return 0;
}
```

Source: TU Berlin, HEVC decoder

OpenCL

- Prog. GPU kernels ✓
- Overhead data trans. ✗
- Prog. model mismatch ✗

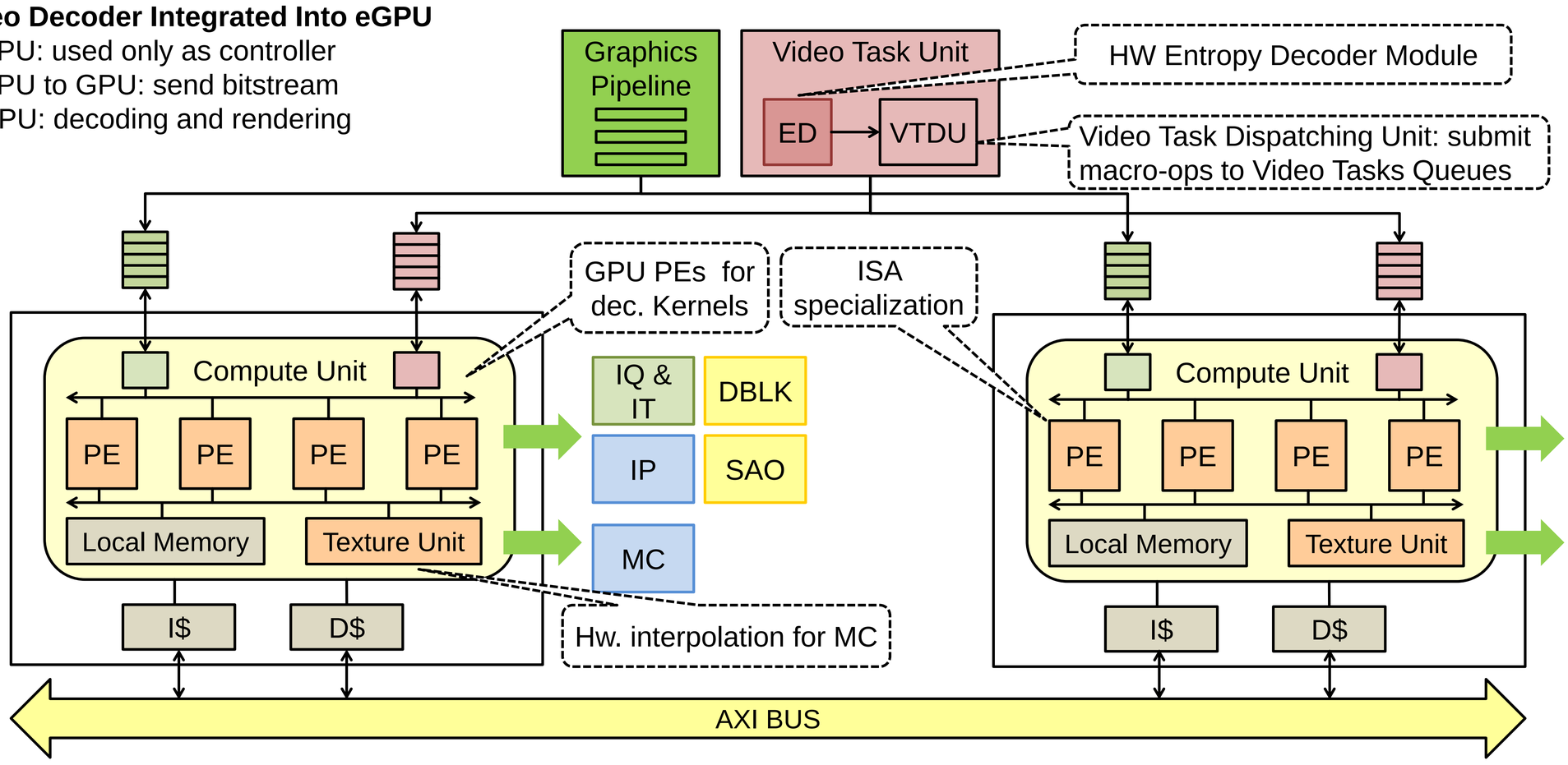


Source: Kronos Group

TTP Solution

Video Decoder Integrated Into eGPU

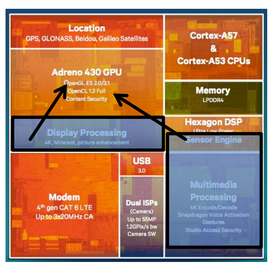
- CPU: used only as controller
- CPU to GPU: send bitstream
- GPU: decoding and rendering



TTP Impact

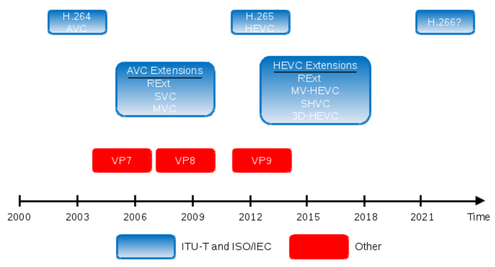
Programmable eGPU Video Decoder

Less area: use GPU cores for video decoding

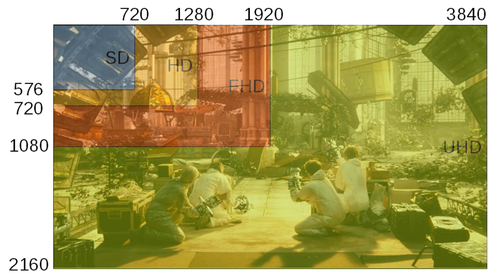


Source: Qualcomm Snapdragon SoC

Extensibility: support multiple codecs



Performance scalability: FHD to UHD



New Products

ThinkSilicon low-power Nema GPU

+

TU Berlin highly optimized H.265 Decoder

Think Silicon mobile GRAPHICS

HEVC High Effecieny Video Coding

New Company

TU Berlin start-up: www.spin-digital.com

TTP Facts

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Duration: 01/09/2014-31/12/2014

Think Silicon

AES Embedded Systems Architecture

Technische Universität Berlin