



FP7 Coordination and Support Action to fund 50 technology transfer projects (TTP) in computing systems. This project has received funding from the European Union's Seventh Framework Programme for research, technological development and demonstration under grant agreement n° 609491.

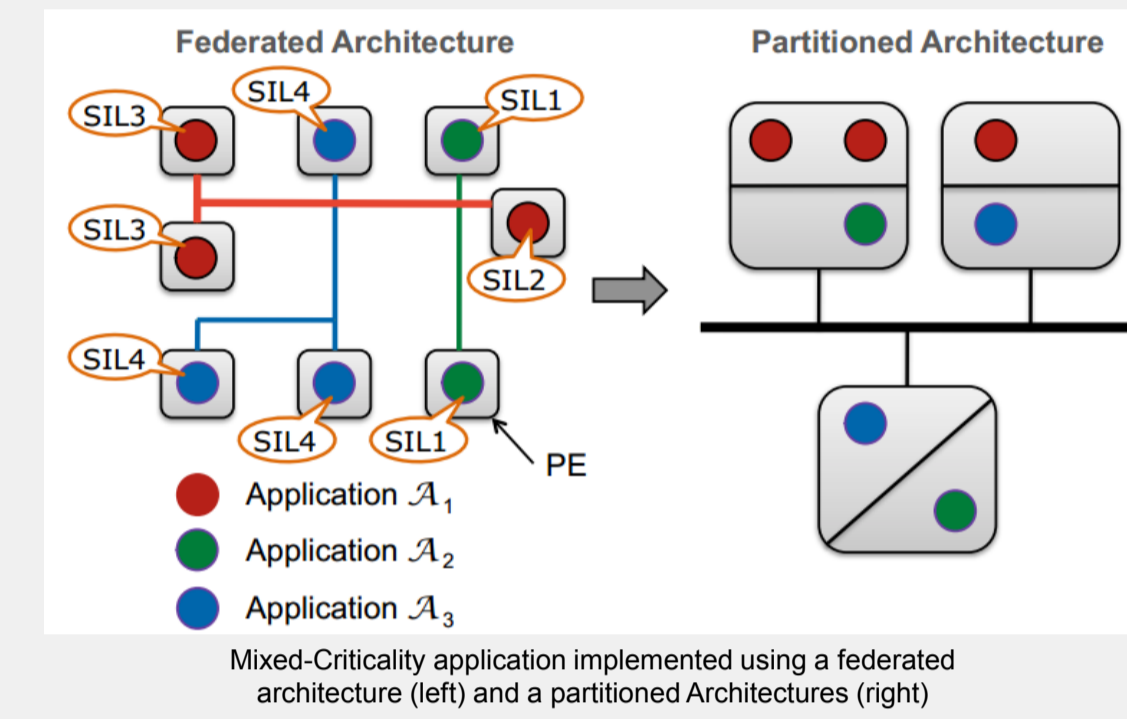
Functionality assignment to partitioned multi-core architectures

Florin Maticu and Paul Pop, Technical University of Denmark
Christian Axbrink and Mafijul Islam, Volvo Group Trucks Technology

TTP Problem

Motivation

- Federated to partitioned architectures
- Multi-core ECUs
- Increase complexity of software functionalities.
- Safety according to ISO 26262
- Schedulability of tasks running of different cores
- Bus bandwidths utilization



Problem Formulation

Given an application model and an architecture model we want to determine :

- A mapping of *software components* to ECUs
- A mapping of *runnables* to cores
- A mapping of *runnables* to *OS-Tasks*
- A mapping of *OS-Task* to *OS-Applications*

Such that we want to minimize:

- The overall communication bandwidth
- The variance of core utilization of the system

Taking into consideration that:

- Mapping constraints, if specified, are satisfied
- The *runnables* are schedulable ($U < 0.69$)
- The *runnables* with different safety integrity levels are spatially and temporally isolated.

TTP Solution

Mapping Optimization

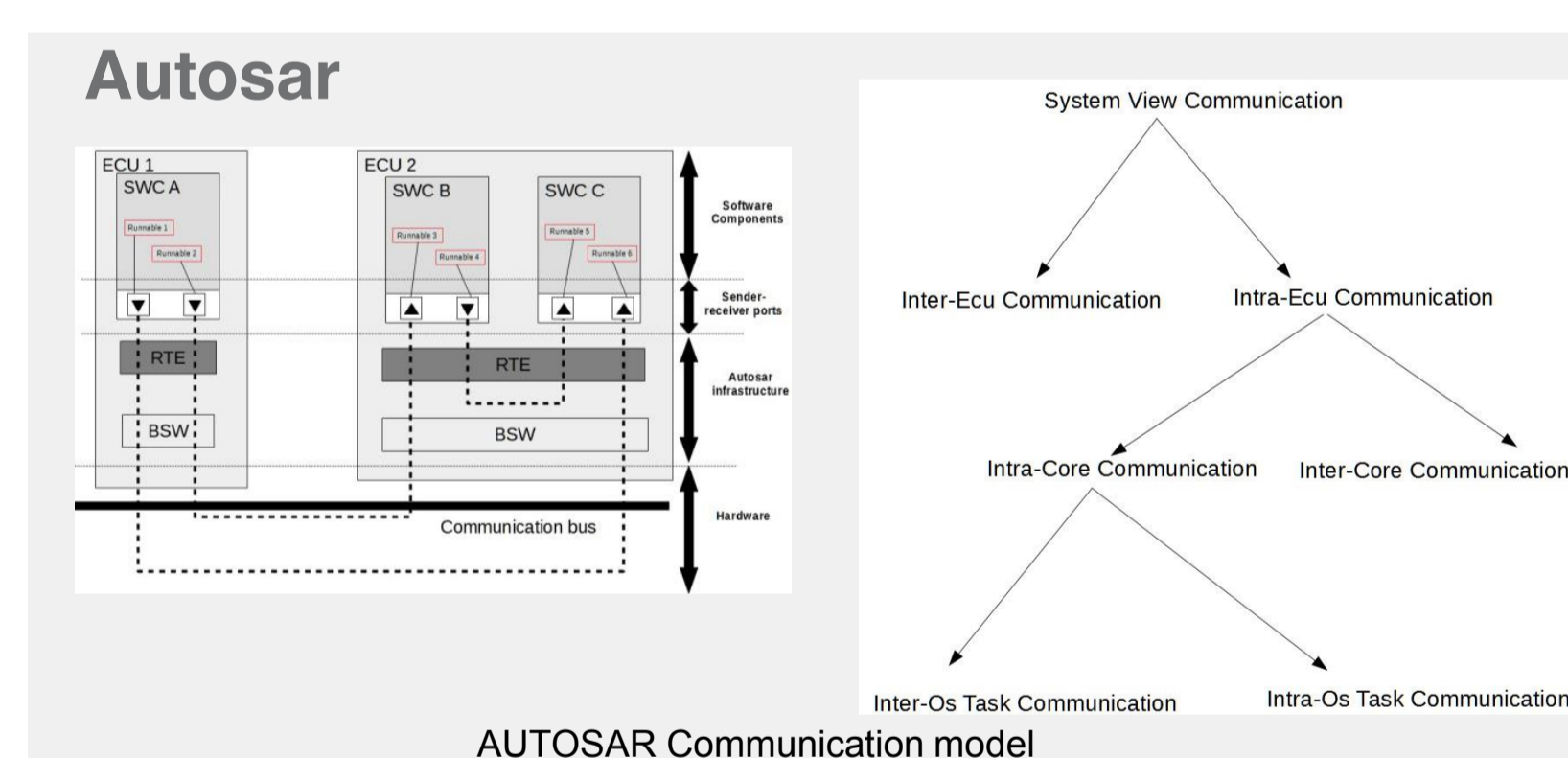
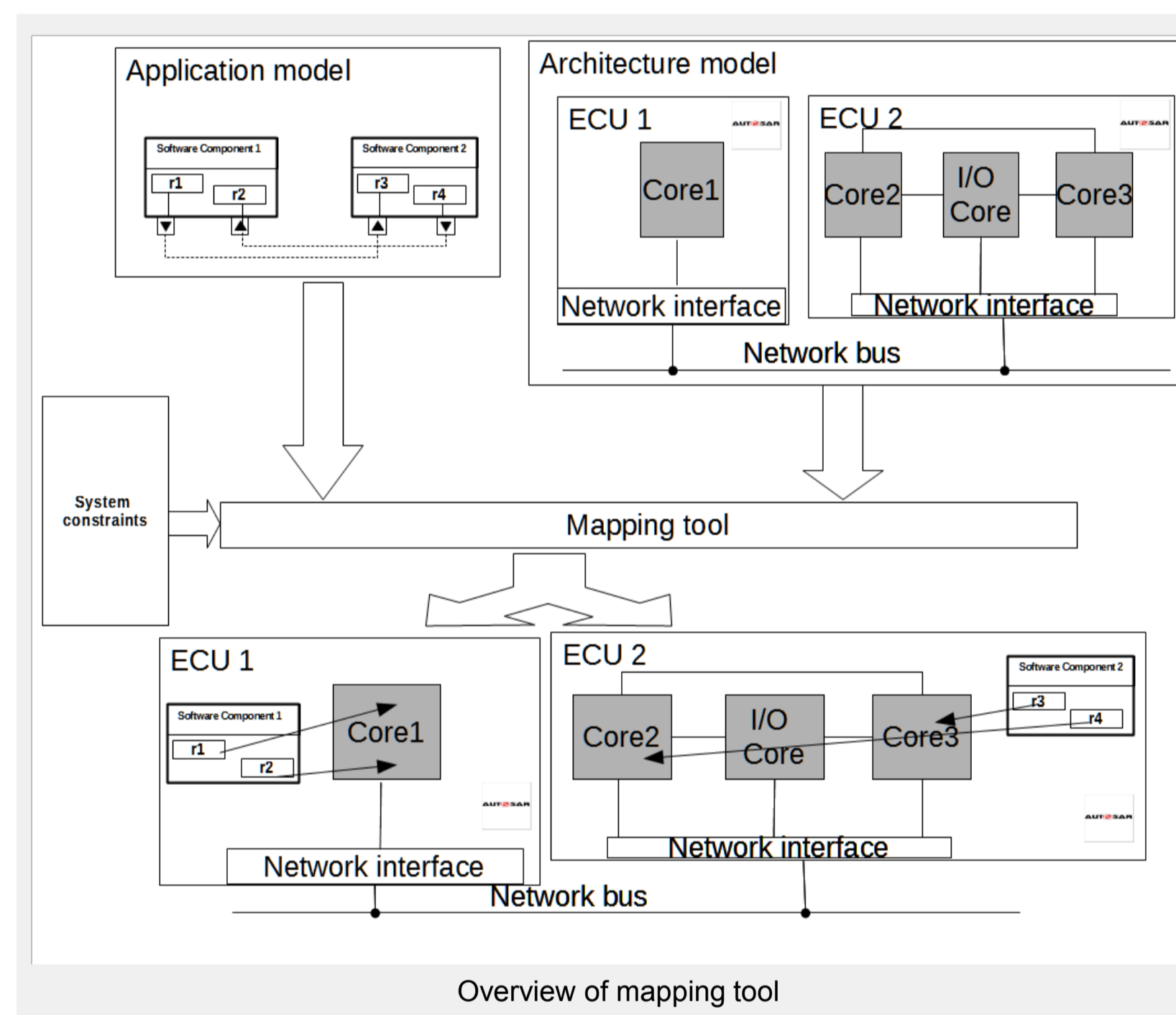
NP-Hard problem, so Simulated Annealing based optimization strategy is used which searches, using transformations, for solutions minimizing a given cost function .

- Cost function:

$$cost = W_1 \times \sigma + W_2 \times U_b + P_1 \times \alpha + P_2 \times \beta$$

Where :

- W_1 and W_2 denotes weights
- P_1 and P_2 denotes penalties
- σ the total *variance* in core utilization
- U_b the aggregated bus utilization
- α denotes the amount of cores which utilization has been exceeded
- β denotes the amount of busses which utilization has been exceeded



Transformation strategies

- Randomly choose a *software component* and map it to a new, randomly chosen, ECU. Then Randomly map the *runnables* inside the *software component* to the cores of the new ECU.
- Randomly choose a *runnable* and map it to a new, randomly selected, core within the same ECU.
- Randomly choose two *runnables* of the same ASIL level assigned to the same core and group them together into an *OS-Task*.

```

Input:
application model
architecture model
system mapping constraints
current temperature, minimum temperature, max steps per temperature
Output:
A mapping of software components to ECUs.
A mapping of runnables to OS-Tasks.
A mapping of OS-Tasks to cores.
A mapping of OS-Tasks to OS-Applications.
1 foreach software component in the application model do
2   randomly assign it to an ECU
3   foreach runnable in the software component do
4     randomly assign it to a Core on the ECU
5   end
6 end
7 Compute current cost;
8 while current temperature > minimum temperature do
9   for step := 1..max steps per temperature do
10    Randomly choose a strategy;
11    Generate new solution from the current solution;
12    Compute new cost;
13    if new cost < current cost then
14      current solution = new solution
15    else
16      Choose a random number r in [0, 1];
17      if r < (old cost - new cost) / current temperature > r then
18        current solution = new solution;
19      else
20        end
21      end
22      current temperature = current temperature * cooling factor
23    end
24 end
  
```

TTP Impact

Expected added value from the technology transfer: Efficient utilization of multicores and compliance with functional safety standard ISO 26262 are among the key business needs and challenges while designing the next generation of architectures for commercial vehicles. This project will contribute significantly to meet these needs by providing an efficient method and tool to harvest the full potential of multicores.

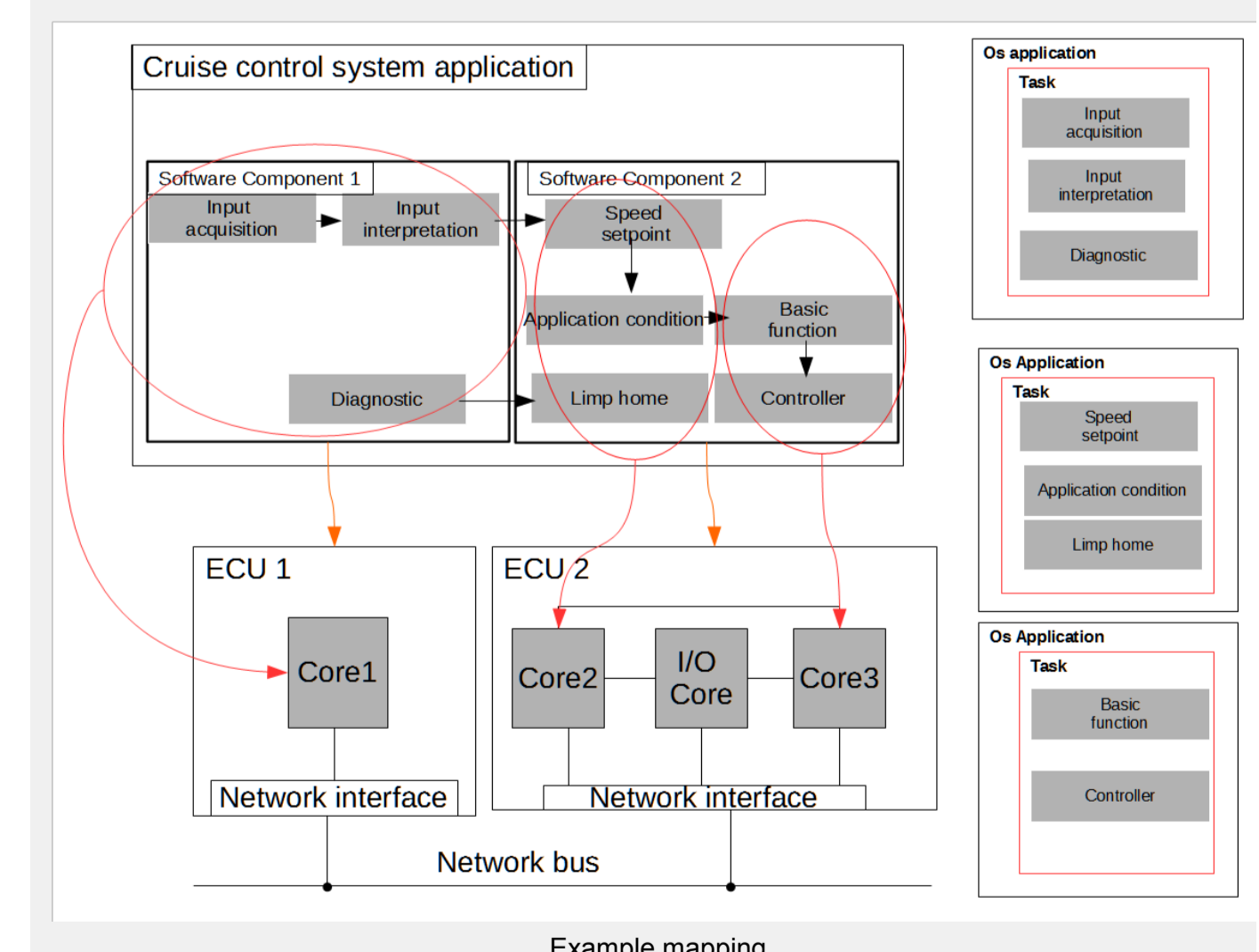
The tool will allow Volvo to reduce the costs (by using multicores and reducing the number of ECUs), maximize performance and resource utilization and handle the increased software complexity.

Volvo Use Case

- Application Model : 50 Software Components with 75 runnables in total.
- Hardware Model : one ECU with 3 cores
- Output within 2 minutes

Example

- Input : Application Model
- Input : Architecture Model
- Output : Mapping



TTP Facts

Contact: Prof. Paul Pop, TU Denmark
E-mail: paupo@dtu.ddk
TETRACom contribution: 20,000 Euros
Duration: 1/2/2016-30/07/2016



DTU Compute
Department of Applied Mathematics and Computer Science

